REMARKS

Claims 1-24 are pending in the present application, claims 25-29 having been withdrawn as being directed to an unelected invention. The Examiner rejected claims 1 and 12 under 35 U.S.C. §112. In addition, claims 1-7, 11-13, 17-20, and 22-24 were rejected under 35 U.S.C. §102, and claims 8-10, 14-16, and 21 rejected under 35 U.S.C. §103. Applicant has amended claims 1, 2, 7, 10, 12, 13, 16, 17, and 19. No new matter has been introduced. By this amendment, Applicant confirms the election of Group I, claims 1-24, and cancels claims 25-29 without prejudice.

Section 112 Rejections

The Examiner rejected claims 1 and 12, and their dependent claims under 35 U.S.C. §112, second paragraph, for being indefinite. Applicant has amended claims 1, 2, 7, 10, 12, 13, 16, and 17 to use the phrases "first memory" and "second memory", as suggested by the Examiner. Reconsideration and withdrawal of these rejections are respectfully requested.

Section 102 Rejections

Claims 1-7, 11-13, 17-20, and 22-24 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 4,569,016 (Hao, *et al.*).

Applicant respectfully traverses these rejections.

In order for a reference to anticipate under section 102, it must disclose, either explicitly, or under the principle of inherency, every claimed limitation of the claimed invention.

Amended Claim 1 recites a method for "aligning and inserting data elements into a first memory" that includes the step of "writing the memory bit lines to the first memory under a control of the mask, wherein said generating and writing steps are performed in response to the single store instruction".

Amended Claim 12 recites a system for "aligning and inserting data elements into a first memory" that includes "means for writing the memory bit lines to the first memory under a control of the mask, in response to the single store instruction".

Claim 19 recites method for "storing data in a memory" that includes "storing a portion of the aligned data within the memory under a control of data type information and an address argument specified by the single store instruction, in response to the single store instruction".

The Examiner cited Hao (col. 13, lines 23-25, col. 18, lines 24-27) as disclosing "writing the memory bit lines to the memory under control of a mask, . . . in response to the single store instruction", and as disclosing "storing a portion of the aligned data within the memory . . . in response to the single store instruction".

Applicant respectfully disagrees.

The section of column 13 cited in Hao discloses a Rotate Immediate then Mask Insert instruction. Although this passage discloses rotating the contents of a register by a predetermined number of positions, and inserting the data into another register under the control of a "generated" mask, there is no positive recitation in this section of "dynamically generating a mask to enable writing of memory bit lines" as part of this instruction, as recited in Applicant's claims 1 and 12. In addition, there is no disclosure of "writing the memory bit lines to the first memory under the control of a mask . . . in response to the single store instruction", as recited in Applicant's claims 1 and 12, in the description of the Rotate Immediate then Mask Insert instruction, or of any other rotate and mask instruction.

The section of column 18 cited in Hao discloses rotate and store instructions. This passage discloses rotating the contents of a register by a predetermined number of bits, generating a mask based on the predetermined of bits, merging the rotated word with the word in another register under control of the mask, and storing the merged word. However, there is no disclosure in this passage of Hao of "aligning the data element in a second memory with respect to a predetermined position in the first memory", as recited in

Applicant's claims 1 and 12, or of "aligning the data . . . relative to a location of the data within a target memory address line", as recited in Applicant's claim 19. Hao merely discloses rotating the register contents by the predetermined number of bits, without disclosing or suggesting that this predetermined number of bits was selected for "aligning the data . . . relative to a location of the data within a target memory address line", as recited in claim 19, or of "aligning the data element . . . with respect to a predetermined position in the first memory", as recited in claims 1 and 12." In addition, column 18 of Hao discloses storing the full merged word is into memory, contrary to Applicant's claim 19 recitation of "storing a portion of the aligned data within the memory . . . ."

Thus, Hao fails to disclose, teach or suggest "aligning the data element in a second memory with respect to a predetermined position in the first memory", as recited in Applicant's claim 1 and 12. Therefore, Applicant urges that Hao does not anticipate claims 1 and 12. Similarly, Hao fails to disclose, teach or suggest "aligning the data in a register relative to a location of the data within a target memory address line" or "storing a portion of the aligned data within the memory", as recited in Applicant's claim 19. Therefore, Applicant urges that Hao does not anticipate claim 19. Reconsideration and withdrawal of these section 102 rejections are respectfully requested.

Claims 2-7, 11, 13, 17-18, 20, and 22-24 all depend from claims 1, 12 or 19, and are thus patentable for at least the same reasons as claims 1, 12 and 19. Reconsideration and withdrawal of these rejections are respectfully requested.

Claims 11 and 24 are patentable for additional reasons. As stated above, column 18 of Hao discloses merging the rotated word with the word in another register under control of the mask, and storing the merged word. Thus, contrary to the Examiner's statement in paragraph 12 of the Action, the rotate and store instruction sequence includes a merge instruction, contrary to Applicant's recitation in claims 11 and 24 of "wherein the instruction sequence is without a merge instruction".

Section 103 Rejections

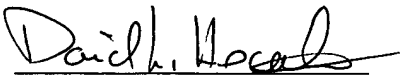
Claims 8-9 and 14-15 were rejected under 35 U.S.C. §103 as being obvious over Hao in view of Applicant's Admitted Prior Art (AAPA). Claims 8-9 depend from claim 1, and claims 14-15 depends from claim 12. AAPA was cited for disclosing a data parity and ECC. However, as stated above, Hao does not disclose, teach or suggest "aligning the data element in a second memory with respect to a predetermined position in the first memory", as recited in Applicant's claim 1 and 12, and the AAPA does not remedy these defects in Hao. Thus, Applicant urges that a *prima facie* case of obviousness of claims 8-9 and 14-15 over Hao and AAPA cannot be maintained. Reconsideration and withdrawal of these rejections are respectfully requested.

Claims 10, 16, and 21 were rejected under 35 U.S.C. §103 as being obvious over Hao in view of U.S. Patent No. 6,167,509 (Sites, *et al.*). Claim 10 depends from claim 1, claim 16 depends from claim 12, and claim 21 depends from claim 19. Sites was cited for disclosing the use of a read-write buffer. However, as stated above, "aligning the data element in a second memory with respect to a predetermined position in the first memory", as recited in Applicant's claim 1 and 12, or "aligning the data in a register relative to a location of the data within a target memory address line" or "storing a portion of the aligned data within the memory", as claimed in claim 19, and Sites does not remedy these defects in Hao. Thus, Applicant urges that a *prima facie* case of obviousness of claims 10, 16, and 21 over Hao and Sites cannot be maintained. Reconsideration and withdrawal of these rejections are respectfully requested.

CONCLUSION

Applicant urges that claims 1-24 are in condition for allowance for at least the reasons stated. Early and favorable action on this case is respectfully requested.

Respectfully submitted,

By: 

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